



1/7

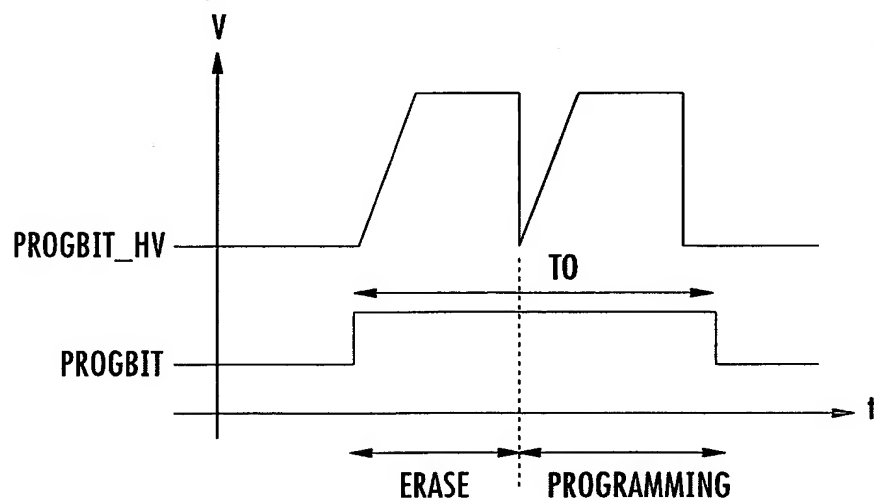


FIG. 1
(PRIOR ART)

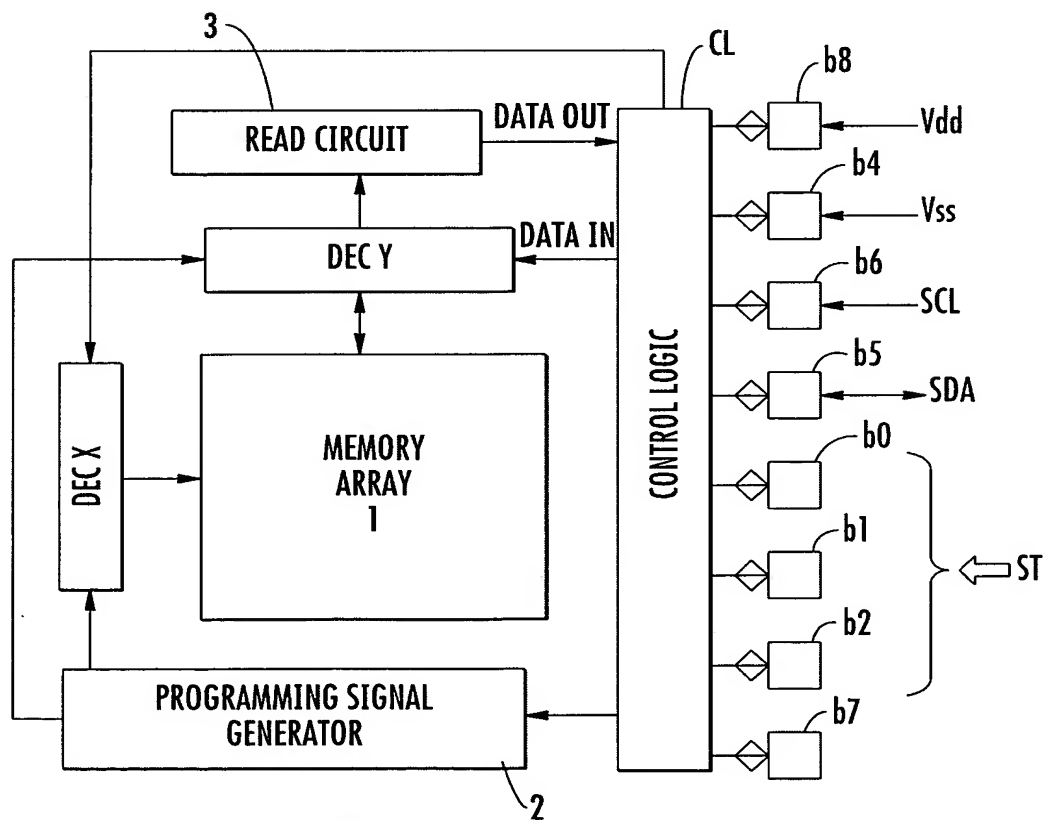
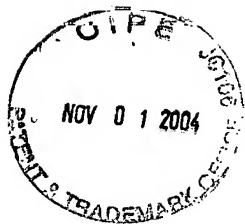


FIG. 4



2/7

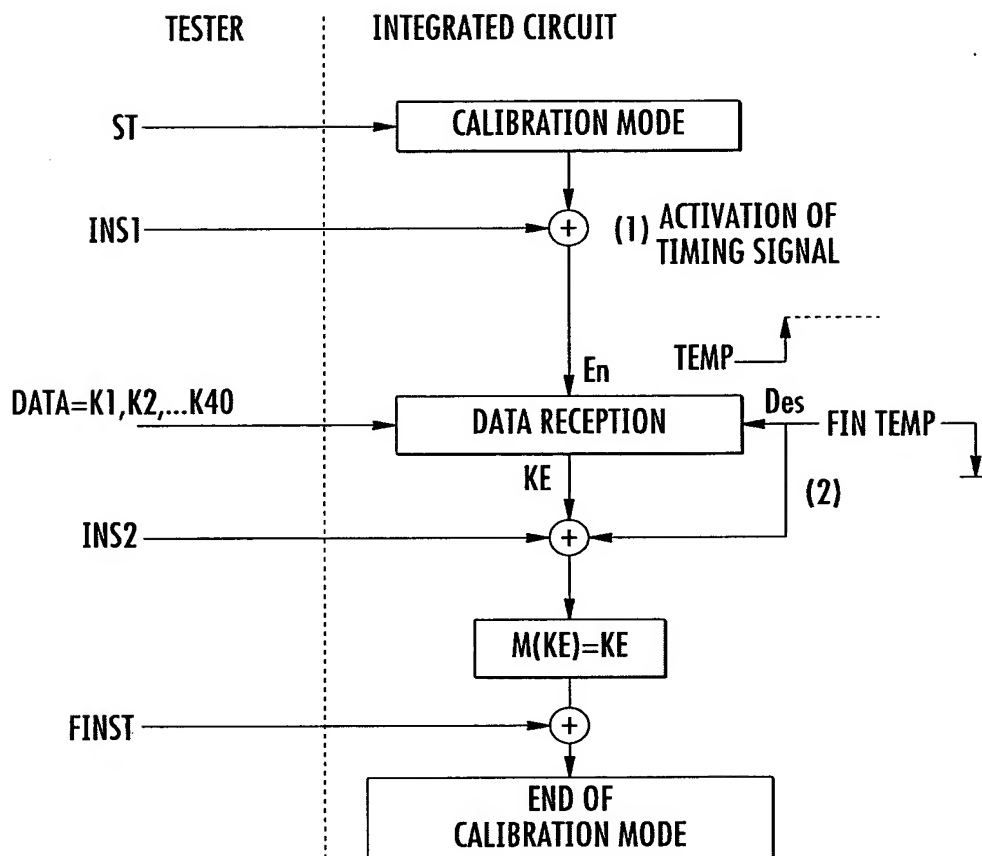


FIG. 2A

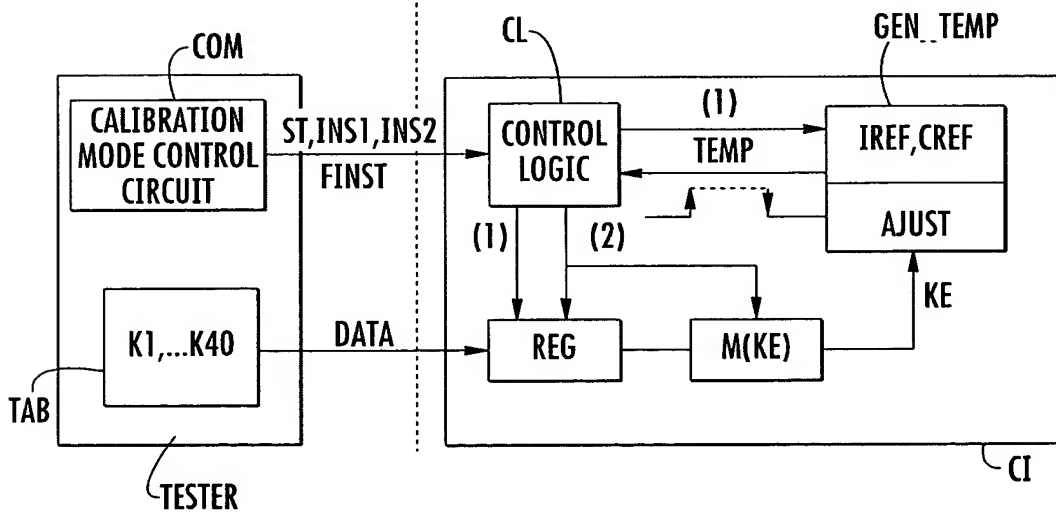


FIG. 2B

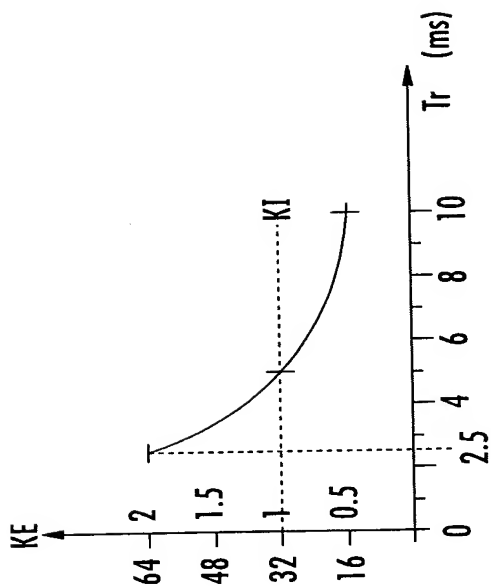


FIG. 3A

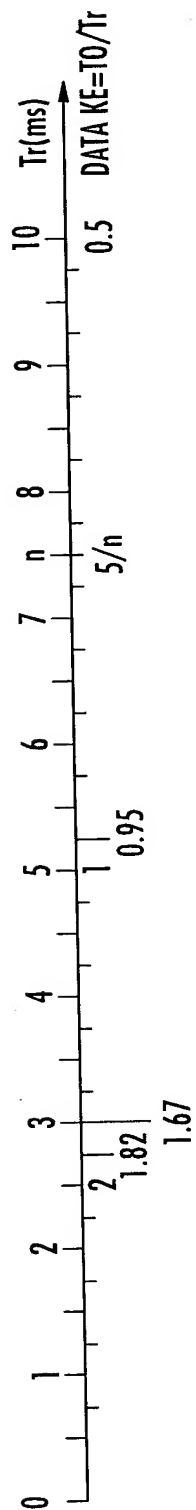
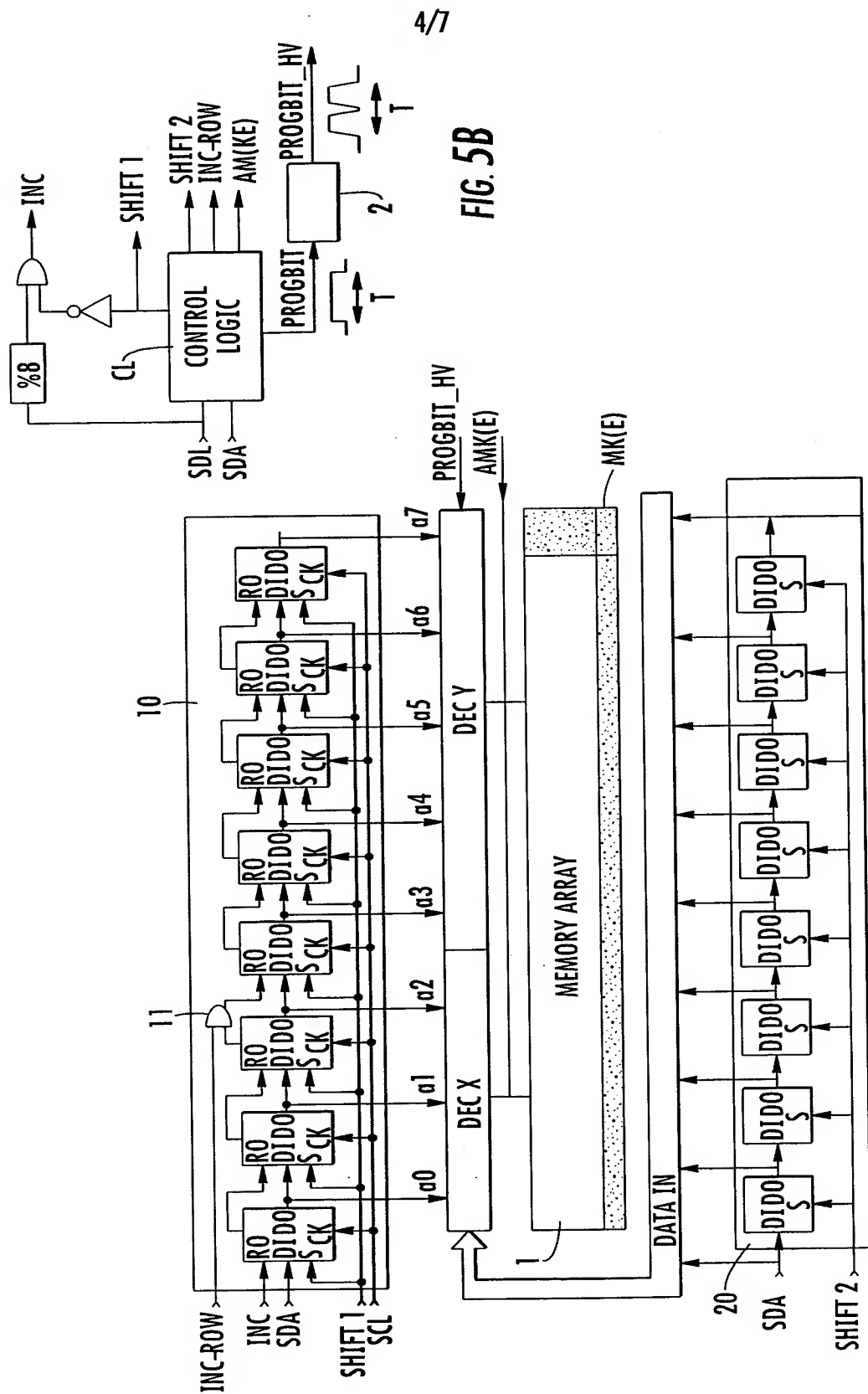


FIG. 3B



4/7

FIG. 5B

FIG. 5A

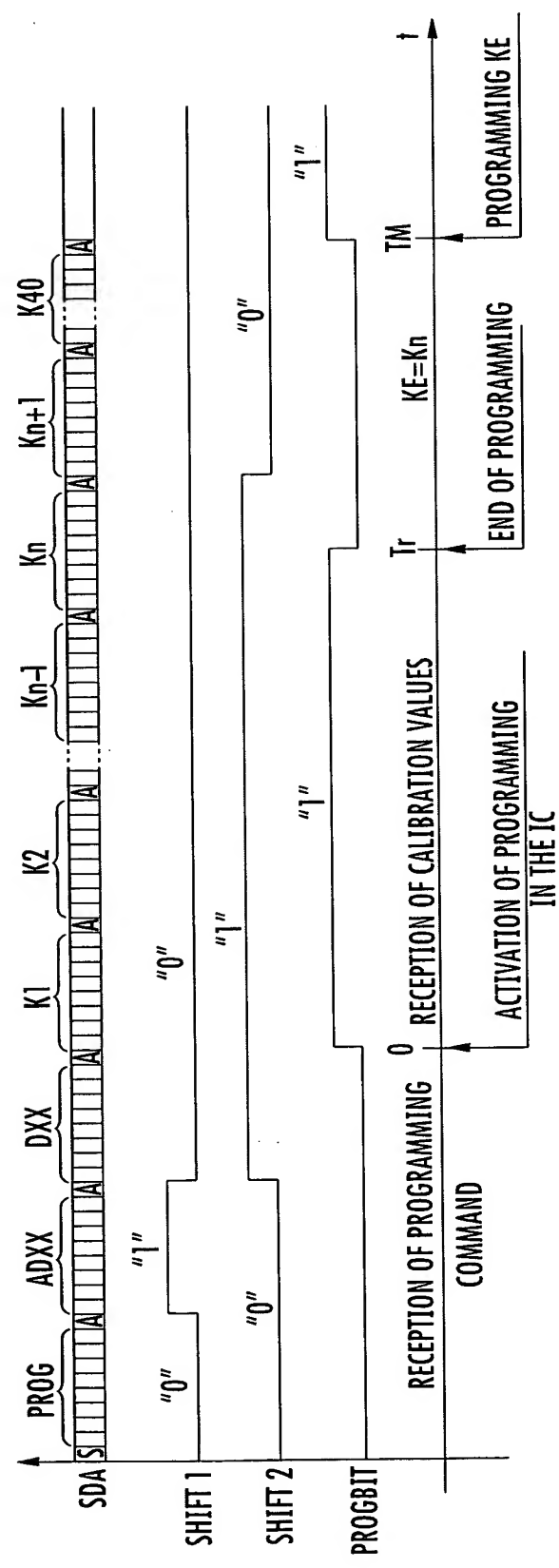


FIG. 6

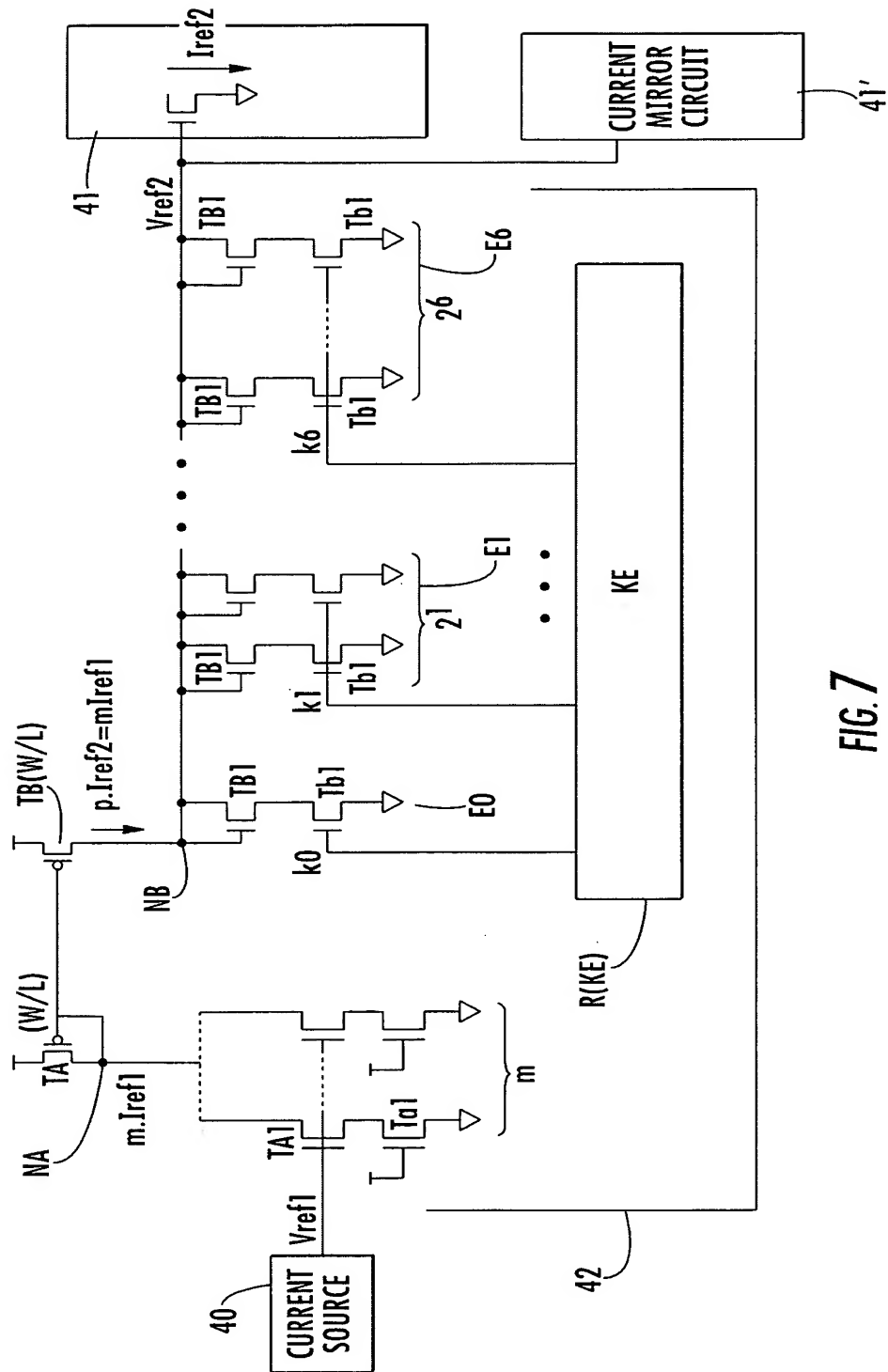


FIG. 7

Figure 1 is a block diagram of a memory array structure. The array is organized into rows, labeled k_0 through k_7 , and columns. A memory array $R(KE)$ is shown, with rows k_0 to k_7 and columns k_0 to k_7 . The array is divided into two sections by a dashed line N . The left section contains sense amplifiers for rows k_0 , k_1 , and k_2 , with a common source line k_3 . The right section contains sense amplifiers for rows k_3 to k_7 , with a common source line k_7 . Each sense amplifier consists of a cross-coupled pair of transistors and a load capacitor C_0 . The output of each sense amplifier is connected to a bus line. A reference voltage $KE.C_0$ is shown at the bottom.